Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) A method for reading and storing data by means of a direct memory access (DMA) medium, comprising the steps of:

determining whether a DMA activation status is set to active for the DMA to perform data transmission;

in the DMA medium, deciding a shift direction and a predetermined number of bits to be shifted in advance when a request is made so that data read from a first storage medium can be processed, if the DMA activation status is set to active; and

sequentially storing bit strings configuring the read data in a DMA control register, shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings to a second storage medium.

2. (original) The method as set forth in claim 1, wherein each of the bit strings configuring the read data is configured by one of an 8-bit string, a 16-bit string or a 32-bit string.

3. (original) The method as set forth in claim 2, wherein the number of bits to be shifted has a value of from 0 to 7.

4. (original) The method as set forth in claim 3, wherein the step of deciding the shift direction and the number of bits to be shifted depends upon bit values set by the DMA medium.

5. (previously presented) The method as set forth in claim 1, further comprising the steps of:

classifying the bit strings configuring the read data into more significant bit strings and less significant bit strings; and

rearranging positions of less and more significant bit strings and writing the bit strings configuring the read data to the second storage medium according to a result of the rearrangement.

6. (previously presented) The method as set forth in claim 5, wherein the bit strings configuring the read data is configured in the form of 32 bits at the step of rearranging the positions of the less and more significant bit strings.

7. (original) The method as set forth in claim 6, wherein the step of rearranging the positions of the less and more significant bit strings depends upon bit values set by the DMA medium.

8. (currently amended) An apparatus for reading and storing data by means of a direct memory access (DMA) medium, comprising:

a first storage medium for storing data read in a source address;

a control register for determining if a DMA activation status is set to active for the DMA to perform data transmission;

the DMA medium for deciding a shift direction and a predetermined number of bits to be shifted in advance when a request is made so that the read data can be processed, sequentially storing bit strings configuring the read data in a DMA control register, shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings, if the DMA activation status is set to active; and

a second storage medium for storing data transferred from the DMA medium.

9. (original) The apparatus as set forth in claim 8, wherein the DMA medium reads each of the bit strings configuring the read data with one of an 8-bit string, a 16-bit string or a 32-bit string.

10. (original) The apparatus as set forth in claim 9, wherein the DMA medium carries out a shift operation according to the number of bits to be shifted that has a value of from 0 to 7.

11. (original) The apparatus as set forth in claim 10, wherein the DMA medium decides the shift direction and the number of bits to be shifted according to set bit values.

12. (previously presented) The apparatus as set forth in claim 8, wherein the DMA medium classifies the bit strings configuring the read data into more significant bit strings

and less significant bit strings, rearranges positions of less and more significant bit strings, and writes the bit strings configuring the read data to the second storage medium according to a result of the rearrangement.

13. (previously presented) The apparatus as set forth in claim 12, wherein the DMA medium rearranges the positions of the less and more significant bit strings when the bit strings configuring the read data is configured in the form of 32 bits.

14. (original) The apparatus as set forth in claim 13, wherein DMA medium rearranges the positions of the less and more significant bit strings according to set bit values.

Claims 15 – 18 (canceled)

19. (previously presented) The method of claim 1, wherein a data packet is generated in a mobile communication system and data is shifted by means of a protocol layer, the method further comprising:

at a second layer, receiving at least one first layer data packet from a first layer and storing said at least one first layer data packet in the first storage medium second layer memory by shifting said at least one first layer data packet by as many bits as indicated by a second layer header;

adding the second layer header in front of said at least one first layer data packet to make a second layer data packet; and

transferring at least one second layer data packet to a third layer,

wherein said second layer header includes control information for said second layer data packet.

20. (previously presented) The method of claim 19, further comprising:

at said third layer, receiving said at least one second layer data packet and storing said at least one second layer data packet in a third layer memory; and

adding cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet.

21. (previously presented) The method of claim 19, wherein the first layer comprises a radio link control (RLC) layer.

22. (previously presented) The method of claim 19, wherein the second layer comprises a medium access control (MAC) layer.

23. (previously presented) The method of claim 19, wherein the third layer comprises a physical (PHY) layer.

24. (previously presented) The method of claim 19, wherein the transfer between the layers is performed by direct memory access (DMA).

25. (cancelled)

26. (previously presented) The method of claim [[25]]19, wherein the shift direction and size of bits to be shifted is decided according to information in a header.

27. (cancelled)

28. (previously presented) An apparatus for generating a data packet in a mobile communication system, the apparatus comprising:

a first layer to transfer at least one first layer data packet to a second layer, said second layer to receive said at least one first layer data packet from a first layer, to store said at least one first layer data packet in a second layer memory by shifting said at least one first layer data packet by as many bits as indicated by a second layer header, to add the second layer header in front of said at least one first layer data packet to make a second layer data packet and to transfer at least one second layer data packet to a third layer,

wherein said second layer header includes control information for said second layer data packet.

29. (previously presented) The apparatus of claim 28, wherein said third layer to receive said at least one second layer data packet, to store said at least one second layer data

packet in a third layer memory and to add a cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet.

30. (previously presented) The apparatus of claim 28, wherein the first layer comprises a radio link control (RLC) layer.

31. (previously presented) The apparatus of claim 28, wherein the second layer comprises a medium access control (MAC) layer.

32. (previously presented) The apparatus of claim 28, wherein the third layer comprises a physical (PHY) layer.

33. (currently amended) The apparatus of claim 28, further comprising a direct memory access (DMA) medium comprising:

a controller to decide a shift direction and a size of bits to be shifted in advance when a request is made;

a memory to receive a data string from a first memory and to store said data string by shifting according to said decided shift direction and said size of bits; and

a controller ~~transfer~~ unit to sequentially transfer said stored data string to a second memory.

34. (currently amended) A method for reading and storing data and generating a data packet, comprising the steps of:

determining whether an activation status is set to active for direct memory access (DMA) to perform data transmission;

deciding a shift direction and a predetermined number of bits to be shifted in advance when a request is made so that data read from a first memory can be processed, if the activation status is set to active; and

sequentially storing bit strings configuring the read data in a register, shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings to a second memory;

wherein the read data is shifted by means of a protocol layer;

said deciding step comprising, receiving, at a second layer, at least one first layer data packet from a first layer and storing said at least one first layer data packet in the second memory associated with the second layer by shifting said at least one first layer data packet by as many bits as indicated by a second layer header; and

said sequentially storing step comprises adding the second layer header in front of said at least one first layer data packet to make a second layer data packet, and transferring at least one second layer data packet to a third layer, said second layer header comprising control information for said second layer data packet.

35. (new) The method as set forth in claim 1, wherein the DMA activation status is set to active when a DMA activation bit is set to 1.

36. (new) The method as set forth in claim 35, wherein the DMA activation bit is set to 1 when the amount of data is large.

37. (new) The method as set forth in claim 1, wherein the DMA activation status is not set to active when a DMA activation bit is set to 0.

38. (new) The method as set forth in claim 37, wherein the DMA activation bit is set to 0 when the amount of data is small.

39. (new) The apparatus as set forth in claim 8, wherein the DMA activation status is set to active when a DMA activation bit is set to 1.

40. (new) The apparatus as set forth in claim 39, wherein the DMA activation bit is set to 1 when the amount of data is large.

41. (new) The apparatus as set forth in claim 8, wherein the DMA activation status is not set to active when a DMA activation bit is set to 0.

42. (new) The apparatus as set forth in claim 41, wherein the DMA activation bit is set to 0 when the amount of data is small.